REMARKS

Claims 15 and 21-23 remain in the application.

Reconsideration is respectfully requested for rejected claims 15 and 21-23 in view of the following remarks.

Claims 15 and 21-23 have now been rejected under 35 U.S.C. 103(a) as being unpatentable over Lin 6,483,147 in view of Armbrust et al. 6,512,292. The Examiner alleges that Lin discloses a semiconductor device comprising a semiconductor body including silicon substrate 12, a silicon oxide layer 34 on substrate 12 for removing heat from MOSFET 42, a silicon device layer 32 overlying silicon oxide layer 34, and a metal layer 38 formed in silicon device layer 34 for removing heat from semiconductor component MOSFET 42 formed in silicon device layer 32. The Examiner notes that Lin does not disclose a silicon oxide layer electrically insulating the metal layer from the semiconductor component. The Examiner refers to Armbrust et al. as disclosing in Fig. 9 a silicon oxide layer 205 electrically insulating metal layer 280 from cooling posts 240 of semiconductor chip structure 200. The Examiner concludes that it would be obvious to form the Lin device having a silicon oxide layer electrically insulating the metal layer from the semiconductor component such as taught by Armbrust et al.

This rejection is respectfully believed to be in error. Previously, the Examiner issued a Final Rejection based on the Lin patent in view of Takahashi et al. 5,475,254. After it was pointed out to the Examiner that in Takahashi et al. the heat generating component is a thin film titanium nitride (TiN) resistor which is not a semiconductor material and is not a semiconductor component, the Examiner withdrew the Final Rejection and issued another Final Rejection mailed October 27, 2003 on Lin taken with Udrea et al. published application 2002/0041003. A Notice of Appeal was filed from this Final Rejection, and after filing Appellant's Appeal Brief, the Examiner withdrew this Final Rejection and has now issued the present Rejection based on Lin in view Armbrust et al.

However, the present Rejection, based on Lin in view of Armbrust et al., is essentially the same as the initial Final Rejection in March 2003 based on Lin in view of Takahashi et al. There, Takahashi et al. were concerned with heat removal from a thin film resistor on a semiconductor substrate and not with heat removal from semiconductor components within the substrate.

In the present Rejection, Lin is taken with Armbrust et al., and Armbrust et al. is like Takahashi et al. in being concerned with heat removal from electrically conductive circuit

members disposed above a substrate, and not with heat removal from a semiconductor component in the substrate. Note Col.2, lines 44-65 where Armbrust describes the invention as a semiconductor chip structure that includes a substrate and at least one electrically conductive circuit member disposed above the first surface of the substrate. In Col. 3, lines 17-21 Armbrust more particularly describes one or more integrated thermal conductors for dissipating heat generated by conductive circuit members, for example wiring levels, disposed above the substrate of the chip structures. To this end, and with reference to Fig.9, cooling posts 240 are disposed within multiple layers 230 above a substrate 210, the layers 230 comprising wiring levels having conductive lines 250 some of which may need to be cooled. (Col. 7, lines 53-66). As further described, a thermally conductive via structure 285 is provided embedded within substrate 210 and forming part of a thermal sink 280 for removal of heat from cooling posts 240.

Thus, like Takahashi et al., Armbrust et al. are concerned not with removing heat from semiconductor components, but rather with heat generated by resistors and conductors above the semiconductor substrate. This is unrelated to the claimed invention, which as defined by independent claim 15 is:

A silicon on insulator semiconductor device comprising:

a) a semiconductor body having a silicon supporting substrate, a silicon oxide layer supported by the substrate, and a silicon layer overlying the silicon oxide layer,

b) a semiconductor component formed in the silicon layer overlying a portion of the substrate in which silicon has been removed by etching, and

c) a metal layer in the portion of the substrate in which silicon has been removed by etching, the metal layer abutting the silicon oxide and **providing heat removal from the component**, the silicon oxide layer electrically insulating the metal layer from the **semiconductor component**. (Emphasis added).

Lin is concerned with the removal of heat from a semiconductor component formed in a silicon layer overlying a portion of a substrate, as specified in claim 15. However, Lin specifically notes that for his purposes, the conductive plug 38 electrically contacts the semiconductor device 32 through a hole in silicon substrate layer 12 and insulation layer 34. Moreover, Lin states that there is poor heat removal for devices on SOI substrates primarily because of the oxide insulating layer (Col. 1, line 49-50). Thus, Lin expressly teaches removal of the oxide insulation layer with the conductive plug extending into the semiconductor device.

The teachings of Armbrust et al, like the teachings of Takahashi et al., are incompatible with Lin as allegedly suggesting the invention as proposed by the Examiner. Armbrust is not concerned with heat generation in a semiconductor device in a silicon layer, but rather with heat generated by conductive circuit layers disposed above the semiconductor substrate of the chip structures. (Col. 3, lines 17-21). Only in applicant's specification is there a teaching of a silicon on insulator semiconductor device in which a metal layer provides heat removal from a semiconductor component while being electrically insulated therefrom by a silicon oxide layer.

It is further noted that in Applicant's divisional patent application serial no. 10/327,479 the Lin et al., Armbrust et al., and Takahashi et al. references were all cited, yet all claims have been allowed over Lin, Armbrust, and Takahashi.

For the forgoing reasons, it is respectfully submitted that claims 15 and 21-23 are patentable under 35 USC § 103(a) over Lin in view of Armbrust et al. The Rejection should be withdrawn, and claims 15 and 21-23 be allowed and the application advanced to issue.

Should the Examiner have any questions or comments concerning the present response, the undersigned attorney requests the opportunity of discussing the response with the Examiner. A telephone call to the undersigned attorney is requested.

Respectfully submitted,
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